0013-4651/2010/157(4)/H443/6/$28.00 © The Electrochemical Society

Fabrication for Cu/Hydrogen Silsesquioxane Damascene Structure by Nanoimprint

Chih-Chieh Hsu[z] **and Fon-Shan Huang**[*]

Department of Electronics Engineering and Institute of Electronics Engineering, National Tsing Hua University, Hsinchu 30013, Taiwan

A simple method for Cu/hydrogen silsesquioxane (HSQ) single damascene fabrication without the conventional chemical mechanical polish process was demonstrated. The 100 nm wide Cu nanowires were fabricated by electron-beam lithography and immersion plating with plating bath $CuSO_4$/HF. The resistivity of the Cu nanowires was 4.8–5.3 $\mu\Omega$ cm after annealing at 400°C for 5 s. The Cu nanowires were transferred onto HSQ by nanoimprint at room temperature with a pressure of 2.2–3.3 MPa. The Cu nanowires were further embedded into the HSQ film to form a Cu/HSQ damascene structure by a simple curing process at 350°C for 10 s. Furthermore, the transferred Cu nanowires were embedded farther in the HSQ film by controlling the curing temperature and time. The topography and cross section of the transferred Cu nanowires on HSQ were examined by a scanning electron microscope. The line-to-line leakage current conduction mechanism of the damascene Cu/HSQ interconnects was studied at various measuring temperatures by a semiconductor parameter analyzer. The phonon-assisted hopping conduction is responsible for the leakage current with a hopping distance of 4.1 Å and a trap level of ~2.87 eV.
 [DOI: 10.1149/1.3301622]

Manuscript submitted June 5, 2009; revised manuscript received December 21, 2009. Published February 25, 2010.

From the International Technology Roadmap for Semiconductors report,[1] planarization is still an important issue for advanced damascene interconnects. Nowadays, the chemical mechanical polishing (CMP) technique is widely used for planarization applications. The common defects associated with the CMP process are corrosion, scratches, remaining metal, peeling, residual slurry, and organic residues. It also gives rise to dielectric degradation and high tooling cost.[2,3] When new materials for conductors, barrier layers, and dielectrics are introduced for future nanodevices, the slurry and stop layer for the CMP process must be investigated to meet surface planarization. Yamada et al.[4] studied the influence of CMP and post-CMP cleaning process on the electrical characteristic of Cu/silicon oxycarbide. Time-dependent dielectric breakdown (TDDB) lifetimes are negligibly dependent on rough Cu surface corrosion, but TDDB with a crevice corrosion defect density of 1.9 cm^{-2} is 10 times shorter than that of a crevice-corrosion-defect-free sample. For post-CMP cleaning, a tetramethylammonium hydroxide-based solution, which does not have a strong oxidized Cu dissolution ability but can remove particles, shows a 10 times longer TDDB lifetime than that of an organic acid cleaning solution when a barrier metal slurry with an inhibitor other than benzotriazole is used. Meanwhile, for a low-*k* dielectric, the dielectric constant of hydrogen silsesquioxane (HSQ) can be adjusted to 1.5–2.2 by applying a solvent and a curing process to the HSQ to control porosity.[5] The degradation of HSQ by the CMP process was observed by Chang et al.[6] They revealed that the dielectric constant of an HSQ film polished with a silicate-based slurry increased from 2.8 to 3.25 and the leakage current became 10 times higher than that without undergoing the CMP process. Chang et al.[7] also reported the degradation of the dielectric characteristic of an HSQ film by the wet stripper, developer, used in conventional lithography to pattern a via or trench in interconnection applications. The alkalinity in the developer causes the hydrolysis of the HSQ film and subsequently forms the Si–OH bonds. It makes the HSQ film easily absorb moisture. After a wet stripper processing, the dielectric constant of the HSQ increased from ~2.8 to ~11 and the leakage current became 10^3 times higher than that of an as-cured HSQ film. Thus, the development of alternative planarization techniques plays a very important role for the long-term solution.

As we know, the nanoimprint is one of the next-generation lithography techniques.[1] In 2006, Schmid et al.[8] demonstrated the nanoimprint lithography for a Cu dual damascene structure. The CMP process was used for planarization. They revealed that the mean resistance of 48 vias with 1 μm^2 area and height ~0.5 μm is 3.15 Ω. Chen et al. demonstrated the transfer of 200 nm wide Au nanowires onto the HSQ film by the hot-embossing imprint.[9] In that paper, the Au nanowires were fabricated on crystalline Si (c-Si) by electron-beam (E-beam) lithography and immersion plating. By taking advantage of the kinks on an amorphous Si (a-Si) surface to provide nucleation sites for Au deposition during immersion plating, smooth and continuous Au nanowires (~100 nm wide) were successfully obtained.[10] Furthermore, Hsu et al. transferred the Au nanowires onto HSQ/Si by nanoimprint and applied a simple post-curing process to form a Au/HSQ damascene structure without the CMP process.[11] So the damascene structure can be fabricated by nanoimprint and by a simple postcuring, an alternative planarization technique.

In this paper, a simple method for the fabrication of a Cu/HSQ single damascene structure without the conventional complicated CMP process was demonstrated. There are two key techniques. First, we utilized the hot-embossing imprint to replace the conventional lithography process. Second, the Cu/HSQ single damascene structure was fabricated by a simple postcuring process, so the degradation of the dielectric induced by conventional CMP, post-CMP process, and developer was absolutely avoided. The benefits of this process include simplicity, high throughput, and low cost. To further investigate the line-to-line leakage current conduction mechanism of single damascene Cu/HSQ interconnects, Cu/HSQ interconnects with width/spacing of 100/100 nm were fabricated. The topography and cross section of the transferred Cu nanowires on HSQ were examined by a scanning electron microscope (SEM). A conductive atomic force microscope (AFM) was used to measure the resistivity of Cu nanowires. The surface roughness of Cu nanowires and of the Cu/HSQ single damascene structure was investigated by an AFM operating in tapping mode. The line-to-line leakage current of single damascene Cu/HSQ interconnects was performed by a semiconductor parameter analyzer (HP-4156).

Experimental

Cu nanowires formed by immersion plating by using a-Si patterned with nanotrench resist.— After RCA-cleaning the n-type Si(100) wafer, the 40/50 nm thick bilayer a-Si/Si_3N_4 was deposited by low pressure chemical vapor deposition. The substrate was spin-coated with a 230 nm thick layer that comprised an E-beam resist DSE1010, C_{60}, and toluene. Then, E-beam exposure at a dose of 10–14 $\mu C\ cm^{-2}$ (Leica Weprint 200 E-beam stepper with beam energy of 40 keV) and development in 2.38% tetramethylammonium hydroxide for 90 s were performed on the samples. The nanotrench pattern with width/spacing ~100 nm/1 μm was obtained. To investigate the line-to-line leakage current conduction mechanism of the single damascene Cu/HSQ interconnects, the resist pat-

* Electrochemical Society Active Member.
[z] E-mail: d935001@oz.nthu.edu.tw

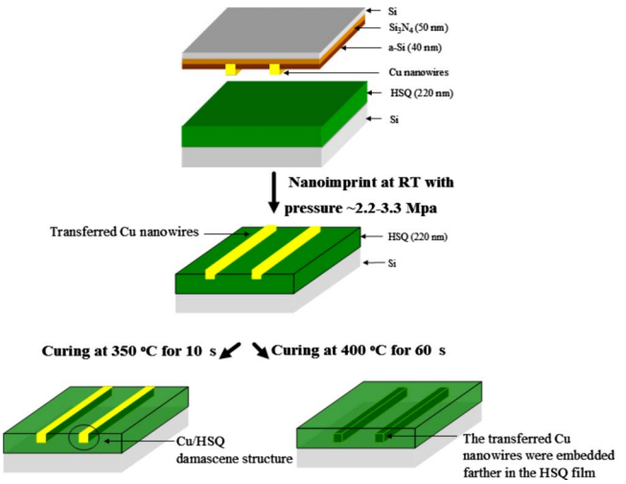

Figure 1. (Color online) Process flow for fabrication of various degrees of embedded Cu nanowires in the HSQ film.

terned with a parallel trench on a-Si with width/spacing ~100/100 nm was also prepared. The plating bath consisted of 11 mM $CuSO_4$ and 1.6 M HF. Then, the sample was immersed into the plating solution for 20 s at room temperature to form Cu nanowires. Immersion copper plating is reported to be a direct redox reaction.[12] Anodic and cathodic processes occurred simultaneously at the Si surface. The Cu ions were reduced by gaining the electrons from Si. Meanwhile, Si was oxidized to form dissoluble species in the presence of F^-.

The half-cell reactions are expressed as follows[12]

anode

$$Si^0 + 6F^- \rightarrow SiF_6^{2-} + 4e^- \quad [1]$$

cathode

$$Cu^{2+} + 2e^- \rightarrow Cu^0 \quad [2]$$

Finally, the resist was stripped by immersing the samples in acetone for 1 min. Thermal annealing of Cu nanowires was performed under flowing N_2 at 400°C for 5 s to promote grain growth. To measure the resistivity of Cu nanowires, the conducting Cu pad (~200 nm thick) was coated on one end of the Cu nanowires by sputter deposition. The total resistance (R_T) of Cu nanowires was measured by an AFM (CP-II, Digital Instruments) operating in contact mode. The detail was discussed in our previous study.[10] The resistivity (ρ) of Cu nanowires can be extracted from the plot of the resistance vs the distance between measurement points and the conducting Cu pad. Tapping mode AFM was used to measure the surface roughness of Cu nanowires.

Single damascene Cu/HSQ interconnects fabricated by nanoimprint.— The detailed process flow for single damascene Cu/HSQ interconnects is shown in Fig. 1. The HSQ (FOX 15, Dow Corning Corporation) diluted with methyl isobutyl ketone (MIBK) was spin-coated on a Si wafer and prebaked at 150°C for 3 min on a hot plate to adjust its film viscosity and hardness. The volume ratio of HSQ/MIBK was 4/5. When the HSQ/Si substrate was prepared, the as-deposited Cu nanowires with width/spacing ~100 nm/1 μm were imprinted onto HSQ/Si by an EVG 520HE at room temperature with an imprinting pressure of 2.2–3.3 MPa. After nanoimprinting, curing at 350–400°C for 10–60 s was applied to the samples by rapid thermal annealing (RTA) to embed the transferred Cu nanowires into the HSQ film. From the SEM images, the optimal condition of planarization was determined. The surface roughness of the Cu/HSQ single damascene structure was obtained by tapping mode AFM.

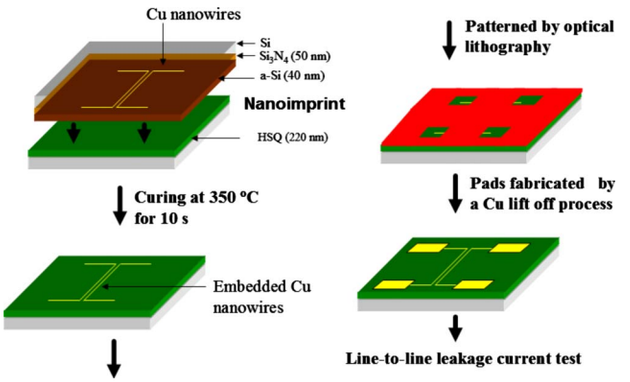

Figure 2. (Color online) Process flow for fabrication of parallel single damascene Cu/HSQ interconnects for line-to-line leakage current conduction mechanism.

The process flow to fabricate the sample used for investigating the line-to-line leakage current conduction mechanism is shown in Fig. 2. The parallel Cu nanowires with width/spacing ~100/100 nm were immersion-plated and annealed at 400°C for 5 s to promote grain growth. They were then imprinted onto HSQ/Si at room temperature with imprinting pressure of 2.2–3.3 MPa. Preventing the diffusion of Cu in the HSQ film, the curing temperature at 350°C for 10 s was chosen to form single damascene Cu/HSQ interconnects. The four conducting Cu pads of 60 × 60 μm^2 were deposited by a Cu lift-off process on the ends of the parallel line with conventional optical lithography. The leakage current was measured by a semiconductor parameter analyzer (HP-4156) on the probe station. To study the temperature dependence of the line-to-line leakage current, the hot chuck was sequentially operated at 25, 50, 100, 150, and 200°C. The dielectric constant of the HSQ film with the above same heat and pressure cycle was monitored by measuring the capacitance–voltage (*C-V*) characteristic of the metal–insulator–silicon capacitor at 1 MHz with a *C-V* analyzer (HP-4294).

Results and Discussion

Cu nanowires formed by immersion plating by using a-Si patterned with nanotrench resist.— Figure 3a shows the SEM plan view of the Cu nanowires with width ~100 nm and height ~70 nm fabricated by immersion plating. It shows that the Cu nanowires are solid and continuous. Because a large amount of sites of low potential energy on the a-Si surface provide suitable sites for Cu nucleation, Cu can easily nucleate on the surface of the a -Si line and further advance into continuous Cu nanowires without voids. The apparent grain size of Cu nanowires is ~10 to 40 nm. Figure 3b shows the SEM plan view of Cu nanowires after annealing at 400°C for 5 s in the N_2 ambient. The apparent grain size is increased

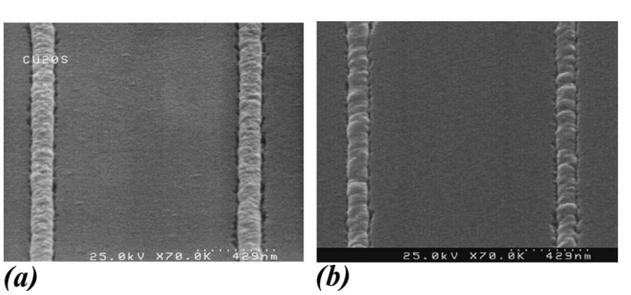

Figure 3. The SEM plan views of (a) as-deposited Cu nanowires and (b) Cu nanowires with annealing at 400°C for 5 s in the N_2 ambient.

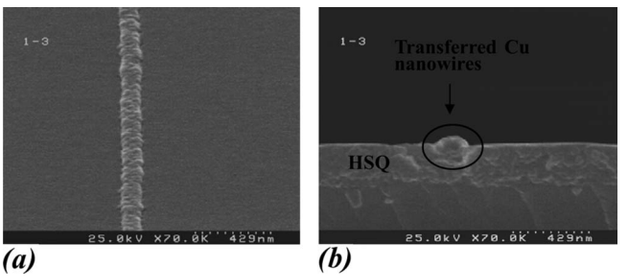

Figure 4. (a) SEM plan view and (b) cross-sectional view of transferred Cu nanowire on the HSQ film.

from ~50 to 100 nm. The surface root-mean-square roughness for as-deposited Cu nanowires and Cu nanowires with annealing at 400°C for 5 s is 5.5 and 4.0 nm, respectively, obtained by tapping mode AFM. To further investigate the resistivity of Cu nanowires, current–voltage characteristics were measured by conductive AFM.[10] The resistivity of the as-deposited Cu nanowire is about 14.5–18.5 $\mu\Omega$ cm. The resistivity of Cu nanowires after annealing at 400°C for 5 s decreased to 4.8–5.3 $\mu\Omega$ cm. This value is higher than that of pure bulk Cu. It might be due to grain boundary scattering, surface scattering, and contact resistance variation in measurements.[10] The values of 6.1 and 3.1 $\mu\Omega$ cm for comparable width of Cu nanowires were reported by Huang et al.[13] and Steinhogl et al.[14]

Fabrication of Cu/HSQ single damascene structure.— Cu nanowires transferred by nanoimprint.— Although the adhesion between Cu and the substrate fabricated by immersion plating is generally poor,[12] it is more proper to transfer them to the low-*k* material, HSQ, for fabricating interconnects. The nanoimprint process was performed at room temperature with pressure of 2.2–3.3 MPa. Figure 4a and b shows the SEM plan view and cross-sectional view of the Cu nanowire with width ~100 nm and height ~70 nm transferred onto the HSQ film. The whole Cu nanowires with length of 100 μm were totally transferred onto HSQ. It gives a high fidelity transfer. The Cu nanowire is imprinted to the depth of ~30 nm without any discontinuity and distortion.

Cu nanowires embedded into HSQ by a simple curing process.— Figure 5a shows the SEM perspective view of the transferred Cu nanowire on HSQ after curing at 350°C for 10 s. It shows that the transferred Cu nanowire is fully embedded into the HSQ film. The embedded Cu nanowire is a continuous and solid line without distortion. The Cu/HSQ interface is distinct. It also shows that a flat surface on Cu/HSQ is certainly obtained after the curing process. The root-mean-square roughness of the surface is 2.4 nm. Figure 5b shows the SEM perspective view of the Cu/HSQ after curing at 400°C for 60 s. It shows that the Cu nanowire is further embedded into the HSQ film to the depth of ~20 nm. The embedded Cu nanowire is also continuous and solid without distortion. For aging study, Fig. 5c shows the SEM perspective view of the sample in Fig. 5a after 5 months of storage in ambient condition. There is no significant change in the Cu/HSQ single damascene structure. It means that the single damascene structure fabricated by this method is stable under ambient conditions. The as-deposited HSQ film generally has a chemical composition of $(HSiO_{3/2})_n$ with a cagelike structure. When the curing process is applied to the film, the Si–H bonds disassociate and the cage structure transforms to a ladderlike network structure.[15,16] In addition, during the curing process, the MIBK evaporates and also leaves porosity in HSQ. The free space resulting from the transformation of the cage to a porous network structure and from the evaporation of MIBK makes the Cu nanowires sink in the HSQ during the curing process. Meanwhile, the dielectric constant of HSQ is decreased by taking advantage of the porosity. Figure 6a and b shows *C-V* curves of the as-prepared HSQ and the HSQ that underwent imprinting process and postcuring at 350°C for 10 s. They give dielectric constants of 2.6 and 2.4, respectively. As we know, Cu diffusion degrades the dielectric material. Thus, the deposition of the barrier layer before imprinting Cu nanowire onto HSQ to suppress Cu diffusion will be our future work.

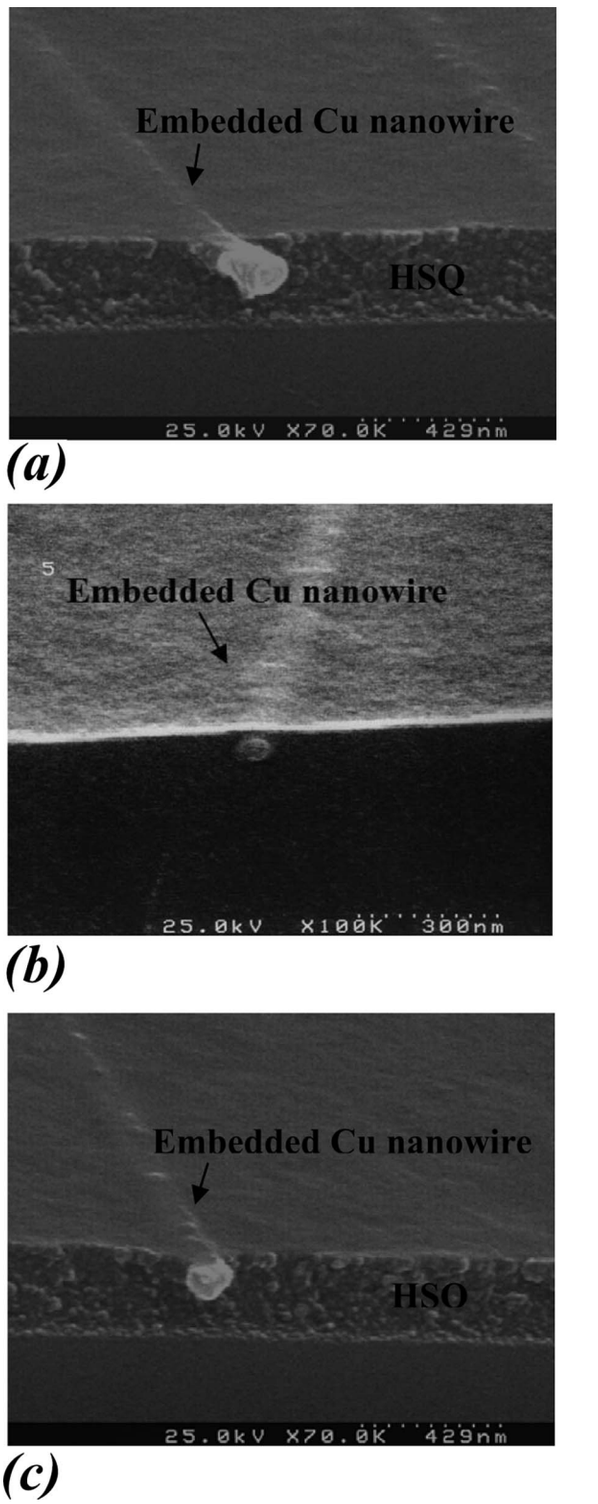

Figure 5. SEM perspective views of Cu/HSQ after curing at (a) 350°C for 10 s and (b) 400°C for 60 s. (c) SEM perspective view of the sample in (a) after 5 months of storage in ambient condition.

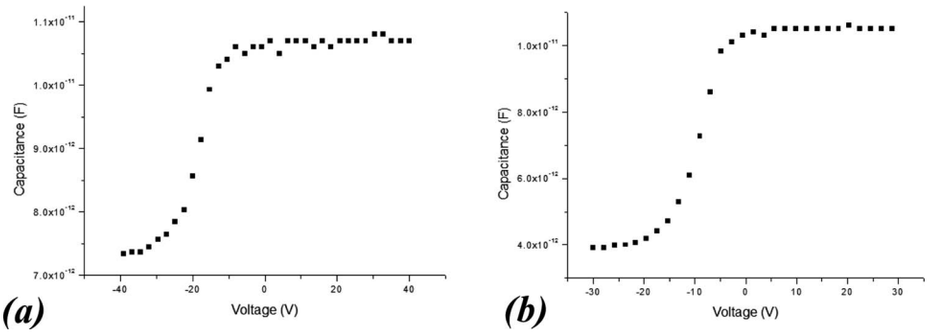

Figure 6. *C-V* curves of (a) as-prepared HSQ and (b) HSQ that underwent imprinting process and postcuring at 350°C for 10 s.

The leakage current study for single damascene Cu/HSQ interconnects.— To study the line-to-line leakage current conduction mechanism of Cu/HSQ interconnects, parallel single damascene Cu/HSQ interconnects were prepared. Figure 7 shows the SEM plan view of Cu nanowires transferred onto the HSQ with width/spacing ~100/100 nm cured at 350°C for 10 s. The probing pads were then fabricated by optical lithography and a lift-off process. Figure 8 depicts the leakage current (I_L) as a function of the applied electric field (E) at measuring temperatures ranging from 25 to 200°C. The leakage current increases with the applied electric field and the measuring temperature.

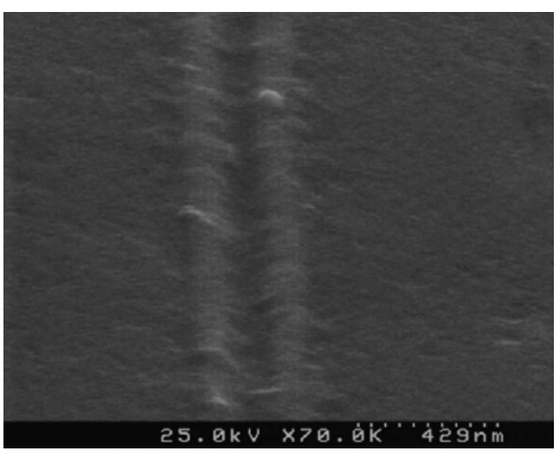

Figure 7. SEM plan view of parallel single damascene Cu/HSQ interconnects fabricated by curing at 350°C for 10 s.

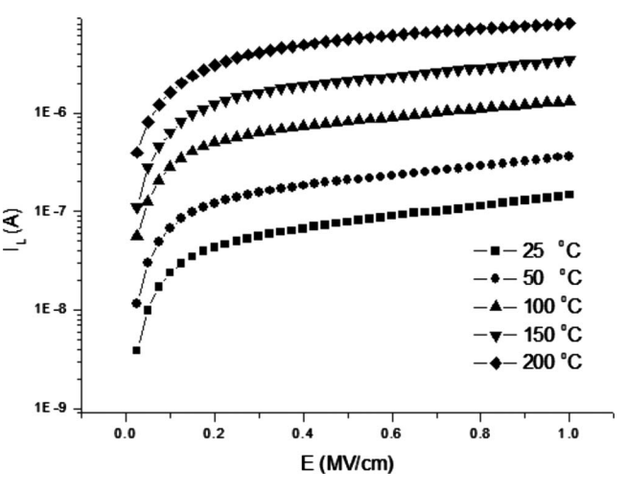

Figure 8. The plot of the leakage current (I_L) vs applied electric field (E) for single damascene Cu/HSQ interconnects.

To investigate the conduction mechanism for the observed leakage current, the Schottky (SC) emission mechanism is used to analyze the measured data first. The current results from the Schottky emission can be expressed as[17]

$$\ln\left(\frac{I_{L,Schottky}}{T^2}\right) = \ln(AA^*) - \frac{1}{k_B T}(\Phi_{BS} - \sqrt{e^3 E/4\pi\varepsilon_0 k_{SC}}) \quad [3]$$

where A is the cross-sectional area, A^* denotes the Richardson constant, k_B is the Boltzmannn constant, Φ_{BS} is the Schottky barrier height at the interface of Cu and HSQ, ε_0 is the permittivity in vacuum, and k_{SC} is the dielectric constant of dielectrics. From Eq. 3, the slope of $\ln(I_{L,Schottky}/T^2)$ vs $E^{1/2}$ is $(1/k_B T)(e^3/4\pi\varepsilon_0 k_{SC})^{1/2}$, which can yield the dielectric constant of the dielectric. The plot of $\ln(I_L/T^2)$ vs $E^{1/2}$ is shown in Fig. 9. It shows that $\ln(I_L/T^2)$ is linearly dependent on $E^{1/2}$ at E ranging from 0 to 0.125 MV/cm and at E ranging from 0.15 to 1 MV/cm with different slopes, respectively. The k_{SC} are 1.1–2.0 and 28–49 at the low and high electric field obtained from the slopes, respectively. Obviously, they are not proper for HSQ films. It means that the Schottky emission mechanism cannot explain the leakage current of the single damascene Cu/HSQ interconnects. The leakage current of the Cu/HSQ interconnects was further examined by the Frenkel–Poole (FP) emission mechanism. The leakage current results from the FP emission can be expressed as[17]

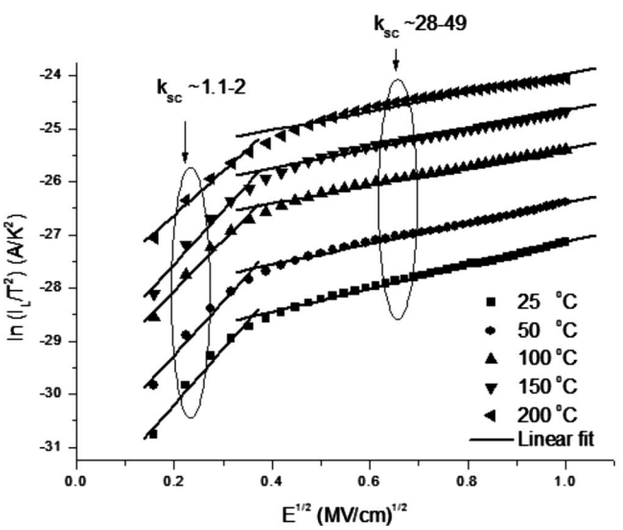

Figure 9. The plot of $\ln(I_L/T^2)$ vs $E^{1/2}$ for single damascene Cu/HSQ interconnects.

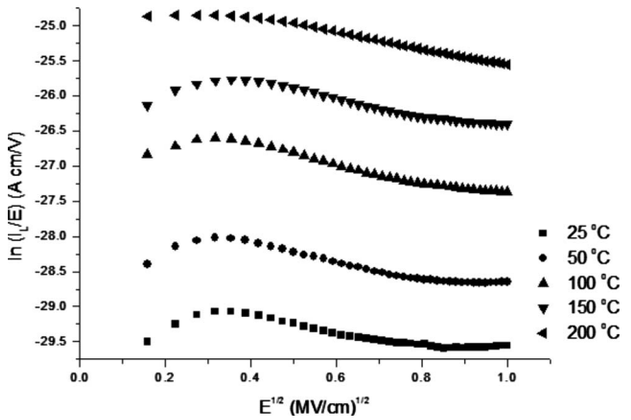

Figure 10. The plot of $\ln(I_L/E)$ vs $E^{1/2}$ for single damascene Cu/HSQ interconnects.

$$I_{L,FP} = BE \exp\left[-\frac{1}{k_B T}(\Phi_{FP} - \sqrt{e^3 E/\pi\varepsilon_0 k_{FP}})\right] \quad [4]$$

where B is a constant, Φ_{FP} is the height of the trap potential well, and k_{FP} is the dielectric constant of dielectrics. Figure 10 plots $\ln(I_L/E)$ vs $E^{1/2}$ for measurement temperatures ranging from 25 to 200°C. From Eq. 4, the slope of the plot is $(1/k_B T)$ $(e^3/\pi\varepsilon_0 k_{FP})^{1/2}$, a positive value. However, the linear fit with a positive slope is not found in Fig. 10. It means that the FP emission is also not responsible for the leakage current of the Cu/HSQ interconnects. The Cu penetration in porous silica shown by a cross-sectional transmission electron microscope image of a Cu/TaN/Ta/porous silica single damascene structure was observed by Shimoyama et al.[18] The diffusivity of a Cu ion in silicon dioxide is $\sim 3 \times 10^{-12}$ cm^2 s^{-1} at 350°C.[19] By a rough estimation, the diffusion distance of Cu is ~ 55 nm for a curing temperature of 350°C for 10 s. Due to the less dense property of porous HSQ, the diffusivity is higher than 3×10^{-12} cm^2 s^{-1}. The penetration of Cu during the curing process degrades the Schottky interface and causes the traps in the HSQ insulator. Thus, the Schottky emission is not observed. Furthermore, the FP mechanism failed to fit the leakage current of the single damascene Cu/HSQ interconnects. For our single damascene Cu/HSQ interconnects, electrons may just hop from one trap state to another trap state to bring about the leakage current. From the phonon-assisted electron hopping theory,[20] the current resulting from the electrons hopping via trap states near the Fermi level can be expressed as

$$I_{L,hopping} = 2AeRk_B TN(E_F)\nu_{ph} \exp(-2\alpha R)\exp\left(\frac{W_t}{k_B T}\right)\sinh\left(\frac{eRE}{k_B T}\right) \quad [5]$$

where e is the electron charge, R is the hopping distance, $N(E_F)$ is the density of states near the Fermi level, ν_{ph} is the phonon frequency, W_t is the trap energy, and $1/\alpha$ is the decay length of the localized wave function. For simplicity, Eq. 5 is simplified by approximation. For a low electric field, $eRE \ll k_B T$, $\sinh(eRE/k_B T)$ can be approximately written as $eRE/k_B T$. Equation 5 then becomes

$$\ln I_{L,hopping} = \ln E + \ln[2Ae^2R^2N(E_F)\nu_{ph}] - 2\alpha R - \frac{W_t}{k_B T} \quad [6]$$

For a high electric field, $eRE \gg k_B T$, $\sinh(eRE/k_B T)$ can be approximately written as $(1/2)\exp(eRE/k_B T)$. Equation 5 then becomes

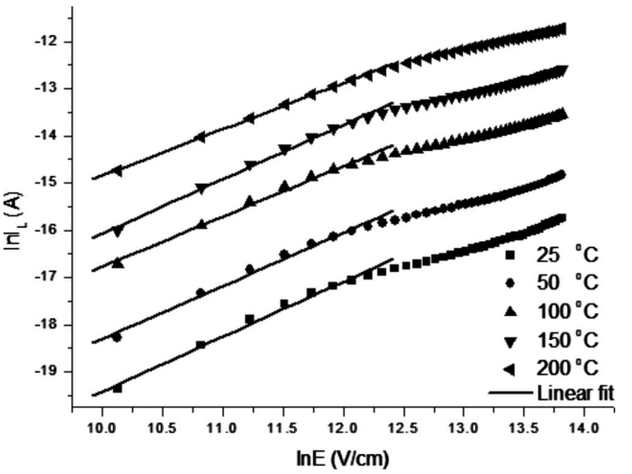

Figure 11. The plot of ln I_L vs ln E for single damascene Cu/HSQ interconnects.

$$\ln\left(\frac{I_{L,hopping}}{T}\right) = \ln[AeRk_B N(E_F)\nu_{ph}] - 2\alpha R - \frac{(W_t - eRE)}{k_B T} \quad [7]$$

Then, the leakage current data are analyzed at low and high electric fields by these approximate equations, respectively. From Eq. 6, $\ln(I_{L,hopping})$ is linearly dependent on ln E with a slope of unity. Figure 11 shows the plot of ln I_L vs ln E. At a low electric field, Fig. 11 shows the linear relationship between ln I_L and ln E with a slope of ~ 0.98 to 1.16. So the leakage current corresponds to the hopping conduction mechanism at low electric field. For a further investigation of the trap level (W_t), the $1/T$ dependence on ln I_L is verified in Fig. 12 (not all the data points are shown in the plot). From Eq. 6, the slope of the plot is $(-W_t/k_B)$, which yields the trap level, W_t, of ~ 0.289 eV.

At a high electric field, the probability of electrons hopping along the field direction would be higher than that of electrons hopping opposite the field direction. Therefore, the current resulting from electrons hopping opposite to the electric field can be neglected. So the last term in Eq. 7 shows this result. From Eq. 7, the slope of $\ln(I_{L,Hopping}/T)$ vs $1/T$ is $(eRE - W_t)/k_B$ denoted as m_H. Therefore, m_H is linearly dependent on E, that is

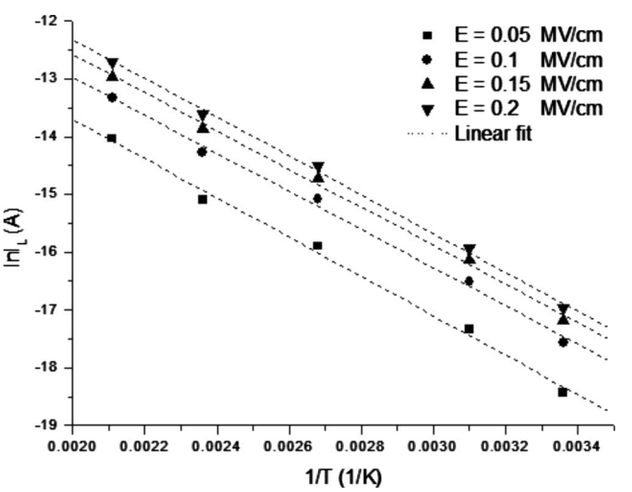

Figure 12. The plot of ln I_L vs $1/T$ for single damascene Cu/HSQ interconnects at low electric field.

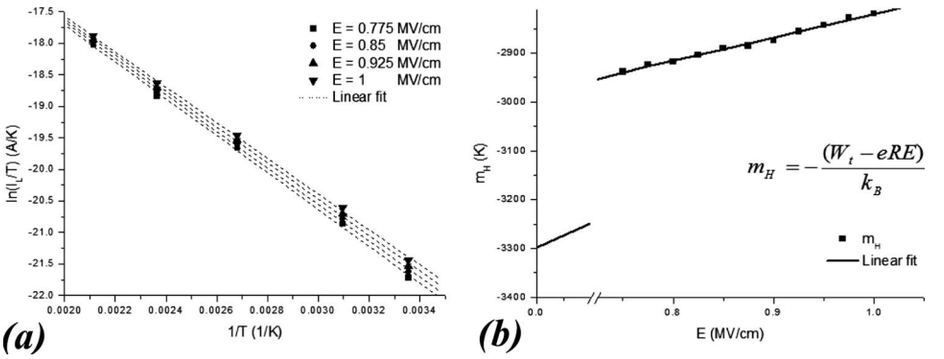

Figure 13. (a) The plot of $\ln(I_L/T)$ vs $1/T$ at high electric field. (b) The plot of m_H vs E.

$$m_H = -\frac{(W_t - eRE)}{k_B} \quad [8]$$

The hopping distance (R) and trap level (W_t) can be further extracted from the slope and the intercept of the m_H vs E plot, respectively. Figure 13a plots $\ln(I_L/T)$ vs $1/T$ for the high electric field of 0.775–1 MV/cm (not all the data points are shown in the plot). Figure 13a shows that the linear fit fits the data for various high electric fields. It confirms that the leakage current of single damascene Cu/HSQ interconnects is dominated by hopping conduction. To further verify the dependence of E on m_H, m_H vs E is plotted in Fig. 13b. m_H does exhibit a linear dependence on the electric field. From Eq. 8, the values of the hopping distance (R), 4.1 Å, and the trap level (W_t), 0.284 eV, can be determined. The trap level of 0.284 eV is consistent with the value of 0.289 eV extracted at a low electric field. Therefore, the electrons hopping via trap states in the HSQ film are responsible for the leakage current of single damascene Cu/HSQ interconnects. When the electric field was further ramped to ~1.5 MV/cm, the electrical breakdown of the Cu/HSQ interconnects was observed.

Conclusions

In this paper, a simple method for the fabrication of a Cu/HSQ single damascene structure by a nanoimprint technique and a simple curing process was demonstrated. Cu nanowires with width of 100 nm and height of 70 nm were fabricated by E-beam lithography and immersion plating. The resistivity of the Cu nanowires after annealing at 400°C for 5 s was 4.8–5.3 μΩ cm. The Cu nanowires were transferred onto the HSQ film by nanoimprinting first. Then the single damascene Cu/HSQ interconnects were successfully obtained by a simple postcuring process at 350°C for 10 s. Meanwhile, the dielectric constant of the HSQ film was decreased from ~2.6 to ~2.4. For the aging study, there was no significant change in the Cu/HSQ single damascene structure after 5 months of storage in an ambient condition. Besides the single damascene structure, the transferred Cu nanowires were further embedded to the depth of ~20 nm in the HSQ film by curing at 400°C for 60 s. The line-to-line leakage current conduction mechanism of the single damascene Cu/HSQ interconnects was also investigated. For simplicity, the leakage current data are analyzed at low and high electric fields, respectively. They both show that the leakage current is dominated by phonon-assisted hopping conduction. The hopping distance (4.1 Å) and the trap level (~0.287 eV) are further extracted from the leakage current data. The breakdown voltage of the Cu/HSQ interconnects is ~1.5 MV/cm. In a future work, the diffusion barrier layer will be integrated in this fabrication process. This work provided a possible candidate for an embedded structure in a future back-end interconnection.

Acknowledgments

This paper was supported by the National Science Council of Taiwan under contract no. NSC 97-2221-E-007-132-MY3 and by the National Nano Device Laboratories under contract no. NDL 97-C05SG-141.

National Tsing Hua University assisted in meeting the publication costs of this article.

References

1. http://www.itrs.net, last accessed May 2009.
2. A. Ishikawa, Y. Shishida, T. Yamanishi, N. Hata, T. Nakayama, N. Fujii, H. Tanaka, H. Matsuo, and T. Kikkawa, *J. Electrochem. Soc.*, **154**, H400 (2007).
3. T. S. Kim, T. Konno, T. Yamanaka, and R. H. Dauskardt, in *IEEE International Interconnect Technology Conference*, IEEE, p. 171 (2008).
4. Y. Yamada, N. Konishi, J. Noguchi, and T. Jimbo, *J. Electrochem. Soc.*, **155**, H485 (2008).
5. H. J. Lee, E. K. Lin, H. Wang, W. L. Wu, W. Chen, and E. S. Moyer, *Chem. Mater.*, **14**, 1845 (2002).
6. T. C. Chang, R. T. Liu, T. M. Tsai, F. S. Yeh, T. Y. Tseng, M. S. Tsai, B. C. Chen, Y. L. Yang, and S. M. Sze, *Jpn. J. Appl. Phys., Part 1*, **40**, 3143 (2001).
7. T. C. Chang, Y. S. Mor, P. T. Liu, T. M. Tsai, C. W. Chen, Y. J. Mei, and S. M. Sze, *Thin Solid Films*, **398–399**, 523 (2001).
8. G. M. Schmid, M. D. Stewart, J. Wetzel, F. Palmieri, J. Hao, Y. Nishimura, K. Jen, E. K. Kim, D. J. Resnick, J. A. Liddle, et al., *J. Vac. Sci. Technol. B*, **24**, 1283 (2006).
9. H. J. H. Chen, J. F. Liu, Y. J. Hsu, J. C. C. Syu, and F. S. Huang, *Nanotechnology*, **16**, 2913 (2005).
10. C. C. Hsu, F. Y. Shen, and F. S. Huang, *Nanotechnology*, **19**, 195302 (2008).
11. C. C. Hsu, L. W. Cheng, and F. S. Huang, in *International Conference on Nanoimprint and Nanoprint Technology Proceedings*, The Japan Society of Applied Physics, p. 42 (2008).
12. L. A. Nagahara, T. Ohmori, K. Hashimoto, and A. Fujishima, *J. Vac. Sci. Technol. A*, **11**, 763 (1993).
13. Q. Huang, C. M. Lilley, M. Bode, and R. Divan, *J. Appl. Phys.*, **104**, 023709 (2008).
14. W. Steinhögl, G. Schindler, G. Steinlesberger, M. Traving, and M. Engelhardt, *J. Appl. Phys.*, **97**, 023706 (2005).
15. Y. Toivola, J. Thurn, and R. F. Cook, *J. Electrochem. Soc.*, **149**, F9 (2002).
16. K. Maex, M. R. Baklanov, D. Shamiryan, F. Iacopi, S. H. Brongersma, and Z. S. Yanovitskaya, *J. Appl. Phys.*, **93**, 8793 (2003).
17. S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, 3rd ed., Wiley Interscience, New York (2007).
18. M. Shimoyama, S. Chikaki, R. Yagi, K. Kohmura, H. Tanaka, N. Fujii, T. Nakayama, T. Ono, A. Ishikawa, H. Matsuo, et al., *J. Electrochem. Soc.*, **154**, D692 (2007).
19. J. D. McBrayer, R. M. Swanson, and T. W. Sigmon, *J. Electrochem. Soc.*, **133**, 1242 (1986).
20. N. F. Mott and E. A. Davis, *Electronic Processes in Non-Crystalline Materials*, 2nd ed., Clarendon, Oxford (1979).